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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
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EXAMINER	
BROCK II,P	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 04/06/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No. 09/609,813	Applicant(s) FORBES ET AL.	
	Examiner Paul E Brock II	Art Unit 2815	

-- The MAILING DATE of this communication appears on th cover sh t with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *48-54* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *48-54* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)
16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 5 .
18) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 51 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 50 states a p-n-p-n-p-n-p planar thyristor. Claim 51 states an n-p-n-p-n-p-n planar thyristor. Claim 51 is dependent from claim 50. It is not clear how claim 51 modifies claim 50 in order to make an n-p-n-p-n-p-n planar thyristor from a p-n-p-n-p-n-p planar thyristor. For purposes of this office action claim 51 will be read to depend from claim 49.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 48 – 50 and 52 – 54 are rejected under 35 U.S.C. 102(b) as being anticipated by Ueno (USPAT 5346838, Ueno).

Ueno discloses in figure 3 a method of forming a circuit for storing information as one of at least two possible stable current states in figures 3 – 6.

With regard to claim 48, Ueno discloses in figure 3 providing a semiconductor substrate (11). Ueno discloses in figure 3 providing doped silicon regions to from a multi-region planar thyristor having at least four regions. Ueno discloses in figure 3 forming at least one polysilicon gate (20) overlying a junction of the multi-region planar thyristor. Ueno discloses in figures 3 and 4 connecting the at least one polysilicon gate to a voltage source (G) in the multi-region planar thyristor. It is inherent that the voltage source is for producing latch-up in the multi-region planar thyristor.

With regard to claim 49, Ueno discloses in figure 3 providing doped silicon regions that form a seven region planar thyristor.

With regard to claim 50, Ueno discloses in figure 3 providing doped silicon regions that form a p-n-p-n-p-n-p planar thyristor.

With regard to claim 52, Ueno discloses in figure 4 the step of providing doped silicon regions further comprises forming two memory cells (CH0 and CH1)

With regard to claim 53, Ueno discloses in figures 3 and 4 connecting a central region of the seven-region planar thyristor to a shared row address line (C).

With regard to claim 54, Ueno discloses in figure 4 the step of providing doped silicon regions further comprises forming one memory cell (CH0).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ueno.

With regard to claim 51, Ueno discloses a p-n-p-n-p-n-p planar thyristor. Ueno does not disclose an n-p-n-p-n-p-n planar thyristor. It is well known in the art to form semiconductor devices of reverse polarity. It would have been obvious to one of ordinary skill in the art at the time of the present invention to form an n-p-n-p-n-p-n planar thyristor in the method of Ueno for design choice of the manufacturer.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Pezzani, Darwish, Bernier et al., Okuhara et al., Temple, Takahashi et al., Kusaka and Okamura all disclose methods of making thyristors formed from implanted regions in a silicon semiconductor device.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E Brock II whose telephone number is (703)308-6236. The examiner can normally be reached on 8:30 AM-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703)308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7722 for regular communications and (703)308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Paul E Brock II
April 4, 2001

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800